MEMS Structural Reliability and DRIE: How Are They Related?

AMFitzgerald & Associates - Tegal Corporation
Webinar and White Paper
Tuesday 27 July 2010

MEMS Structural Reliability and DRIE: How Are They Related?

Summary
Silicon deep reactive ion etch (DRIE) using the time-multiplexed Bosch etching process is an essential MEMS fabrication process technology that has enabled routine formation of the high-aspect ratio microstructures characteristic of MEMS devices such as accelerometers, gyroscopes, and microphones. The Bosch process deep silicon etch generally leaves behind a characteristic scalloped sidewall, with features (sidewall roughness) that can range in depth, peak-to-trough, from nanometers to microns deep. Process engineers frequently go to great efforts to develop etch recipes that minimize sidewall roughness, because conventional wisdom has it that smoother etched surfaces in deep silicon structures typically exhibit higher fracture strengths. But how smooth is smooth enough to make a MEMS device reliable?

In this whitepaper, AMFitzgerald & Associates and Tegal Corporation share the results of their collaborative study performed to characterize and understand the relationship between DRIE sidewall features and the fracture strength of etched silicon structures. Three different silicon DRIE recipes with distinct sidewall roughnesses were used to etch three batches of four-point-bend specimens. The specimens were loaded to fracture and the strength distribution of each surface type was characterized using Weibull analysis. We present our thoughts on the utility of this data for assessing fitness of an etch recipe for a particular MEMS application, for monitoring process stability and tool performance during volume production and for providing valuable empirical data for fracture prediction methods.

Motivation for This Study

Bosch process etching of silicon structures is an integral part of device fabrication for the many MEMS devices currently in commercial high volume manufacturing, such as: two- and three-axis accelerometers for consumer and industrial applications; silicon gyroscopes for consumer electronics and for anti-rollover systems and vehicle stability control in the automotive market; pressure sensors for tire pressure monitoring and for medical instrument applications; inkjet print heads for desktop color printing; image sensors for visible and infrared imaging applications; and electro-acoustic filters for cell phone handsets and other wireless communication applications.

Added together, these commercial MEMS devices total up to billions of units shipped per year by companies that include Hewlett-Packard, STMicroelectronics, Robert Bosch, Avago Technologies, Analog Devices, Seiko Epson, Denso, and Tronics.

The Bosch process is also used in several semiconductor IC fabrication processes, including deep silicon trench isolation in Power Device fabrication, and for creating three-dimensional capacitors for passive devices like electrostatic discharge (ESD) protection circuits, and also for 3D-IC structures using Through Silicon Via (TSV) technology.

Over recent years, silicon DRIE plasma etch tool makers have made great progress increasing etch rates for any given exposed area of silicon. Increases in silicon etch rates for silicon DRIE applications generally results in higher wafer throughputs, and therefore, lower processing cost per wafer. For silicon DRIE tools based on Inductively Coupled Plasma reactors, process and hardware improvements, for example higher power ICP sources, higher gas throughput, and better wafer temperature control, have resulted in a 3X to 4X increase in effective silicon etch rates over the space of five years.

But, beyond pure silicon etch rates, Bosch process etching of MEMS structures must also be optimized for sidewall profile and sidewall smoothness.

Figure 1 is a SEM micrograph of an etched silicon feature, in cross-section, showing the sidewall “scallops” characteristic of Bosch process etching.

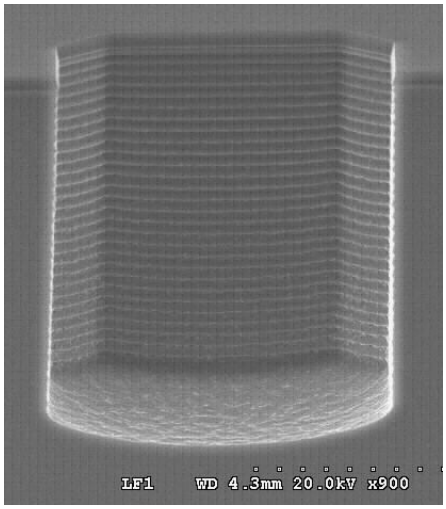


Fig. 1 SEM micrograph of etched silicon feature showing characteristic Bosch process scallops.

Achieving the right amount of sidewall roughness in deep silicon etching is a matter of balancing the etching and passivation sequences in the time-multiplexed (Bosch process) silicon etch process recipe. But, with all ranges of sidewall smoothness possible, how should one choose the optimal recipe for their application?

Conventional wisdom has it that smoother etched silicon surfaces typically exhibit higher mechanical fracture strengths. But how does the fracture strength of silicon-based MEMS devices etched using the Bosch process actually vary with sidewall profile? AMFitzgerald & Associates and Tegal Corporation defined, performed, and analyzed the results from a well-controlled experiment in order to understand more about just that question.

The Bosch DRIE Process

Silicon etches readily in plasma reactors running fluorine-based (e.g. SF6, CF4) etch chemistries. The most widely used fluorine-based etch process for deep silicon etching is a cyclical (or time-multiplexed) process of alternating etch (with SF6, or other fluorine-rich reactant gases) and deposition of a passivation layer (with C4F8, or other polymer-forming gases) steps known as the Bosch process: [1]

Figure 2 illustrates the cyclical principle of the Bosch process for creating a deeply etched feature into silicon.

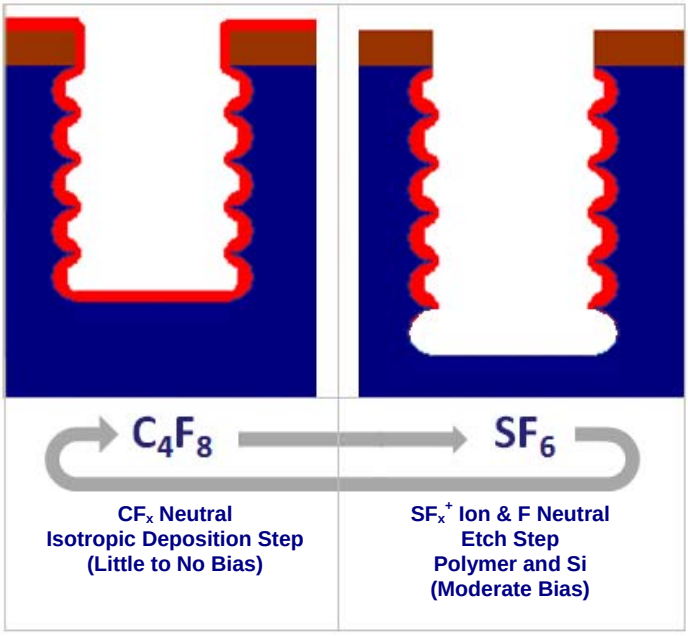
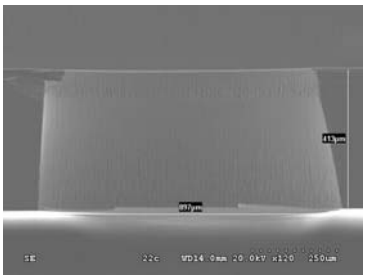
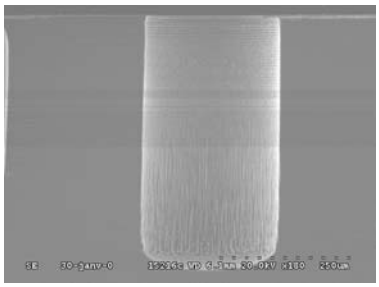


Fig. 2 Cyclical nature of Bosch process etching

Table 1 summarizes some typical Bosch process silicon etch performance for low aspect ratio (Etch Depth / Etch Width; here, typically, < 3:1) MEMS structures such as silicon microphones and inkjet printheads, depicted below.

Table 1: Typical Bosch Process Etch Results – Low Aspect Ratio MEMS Structures in Silicon

		
	Silicon Microphone	**Inkjet Printhead**
Silicon Etch Rate	13µm/min	24µm/min
Etch Depth	400µm	485µm
Etch Width	870µm	250µm
Selectivity to Mask	> 100:1 (PR Mask)	> 150:1 (PR Mask)
Etch NonUniformity	<±4%	<±5%
Exposed Silicon Area	>35%	<10%
Process Regime	Room Temperature	Room Temperature
Aspect Ratio	0.5:1	1.9:1

Achieving the right silicon etch rate and the right amount of sidewall roughness in deep silicon etching is a matter of balancing the etching and passivation sequences. [2] The silicon etch rate is also quite sensitive to pattern loading (defined as the % area of exposed silicon to the plasma). DRIE recipes typically need to be tuned to specific patterns in order to achieve maximum etch performance.

Figure 3 presents the characteristic relationship between silicon etch rate (controlled by the relative amount of time the time-modulated silicon etching process spends in any single etch sequence) and scallop depth. In general, deliberately producing a smooth-sidewall etch result (i.e. sidewalls with shallow scallops) requires implementing etch processes with slower overall silicon etch rates. This means that the price of smooth sidewalls must be traded against the cost of low wafer throughput. For high volume manufacturing, reduced wafer throughput has a very real effect on cost of production, to the point where it could require installation of additional tools just to keep up with

production demand. The value of a smooth sidewall should therefore be carefully assessed from both a technical and business standpoint.

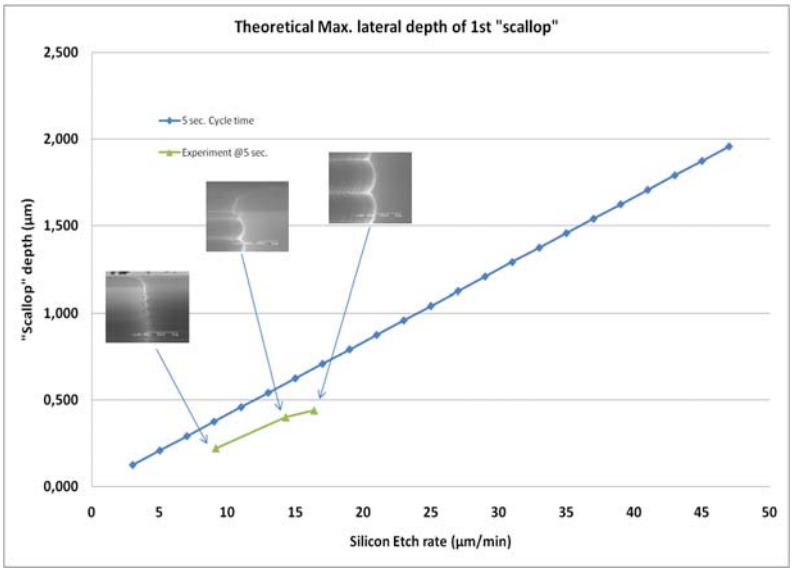


Fig. 3 Scallop depth (sidewall roughness) versus silicon etch rate for a time-multiplexed silicon etch process.

Figure 4 shows a Tegal 3200 DRIE cluster configuration plasma etch tool for MEMS fabrication in which one (of a possible three total) silicon DRIE ICP process module has been installed.

Fig. 4 Silicon DRIE ICP reactor mounted in Tegal 3200 plasma etch system.

How MEMS Structural Reliability and DRIE are Related: Brittle Material Properties

Single crystal silicon wafers are one of the purest and most flaw-free materials manufactured. During the act of etching a MEMS structure from silicon, plasma damage flaws are created all over its surface. Bosch-etched sidewalls have a broad size scale of etch-induced flaws, ranging from the micron-scale scallops to nanometer-scale flaws such as plasma pitting and dangling surface bonds.

MEMS are mechanical devices, so their successful operation depends on their ability to reliably handle structural loading. The load at which a brittle structure fails depends on two variables: the stress developed as a result of the load *and* the population of material flaws present in or on that structure. In ductile materials, such as metals, plastic deformation in the high stress area around flaws minimizes their ability to grow in size. But brittle materials do not have this self-protecting response to stress, so when the stress intensity in the vicinity of a critically-sized flaw exceeds the fracture toughness of the material, catastrophic failure occurs almost instantaneously (something which we've all experienced when dropping a glass on the floor). The principles of fracture mechanics dictate that the strength of a brittle structure (or the maximum stress it can handle before shattering) is a function of flaw size, as shown in Figure 5. This relationship describes why smoother surfaces exhibit higher strengths than rough ones. It also explains why the strength of a brittle structure appears to be random – because the strength is dependent on flaws, which are randomly distributed in the material.

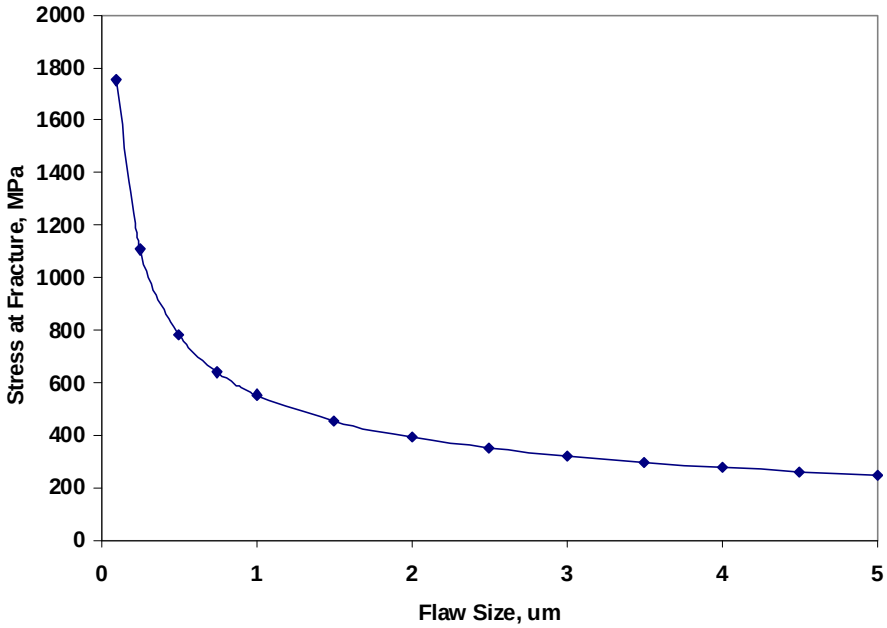
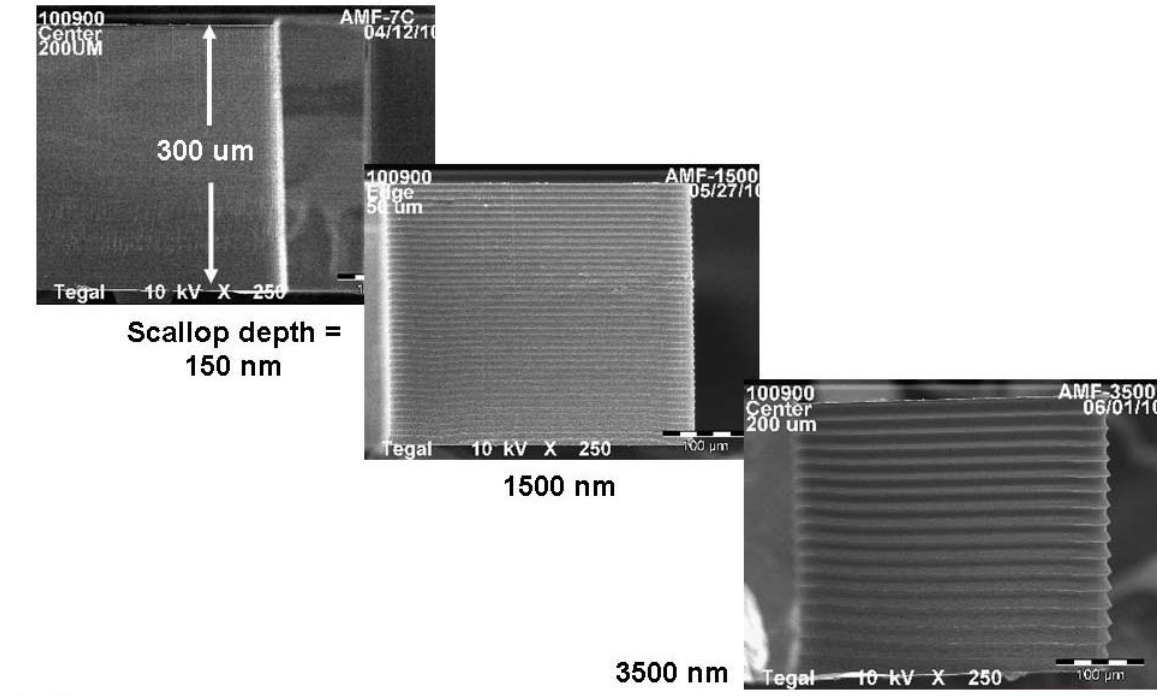


Fig. 5: The fracture toughness relationship between the length of a flaw (crack) and the maximum theoretical fracture strength of silicon in pure tension loading (Mode 1). The fracture toughness, K_{IC}, of silicon is ~ 1.0 MPa-$m^{1/2}$.

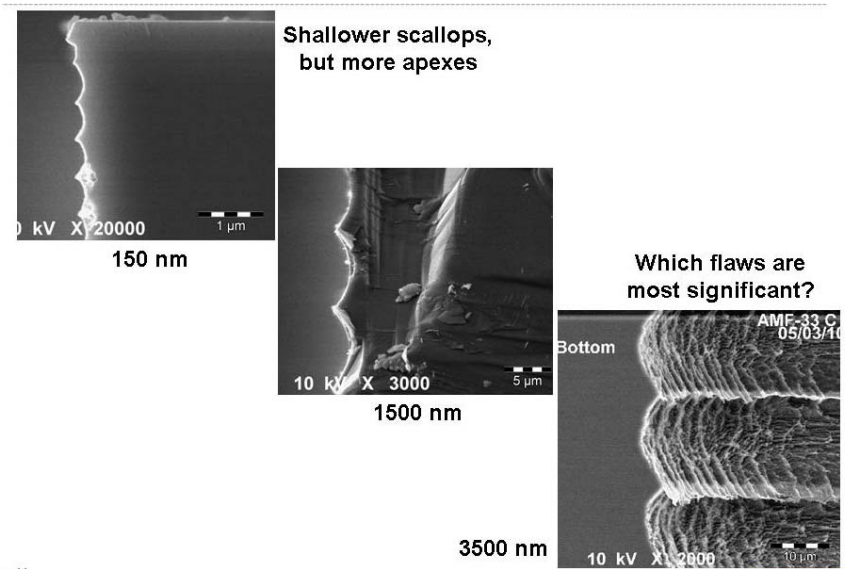
Fracture Strength of Three DRIE Recipes

In theory, we could make stronger MEMS devices, if only we could make the etched surface of the silicon as smooth and flaw-free as possible. While there are techniques for smoothing out etch-induced flaws in silicon (such as 1000ºC hydrogen annealing, or with isotropic etchants), these are usually not practical from a process, thermal budget or cost standpoint. As mentioned above, DRIE process parameters can be adjusted to make smoother sidewalls, but with a corresponding cost in wafer throughput and development time. The question remains, how smooth is smooth enough?

In this study, we set out to measure the strength of surfaces etched by three different DRIE recipes by doing fracture tests. We took a Tegal DRIE etch recipe, and by changing only the etch and passivation times (gas flow rates, pressure and temperature were held constant), achieved three very different sidewall surfaces, with peak-to-trough scallop sizes of 150nm, 1500nm and 3500nm, respectively (Figure 6).



(a)

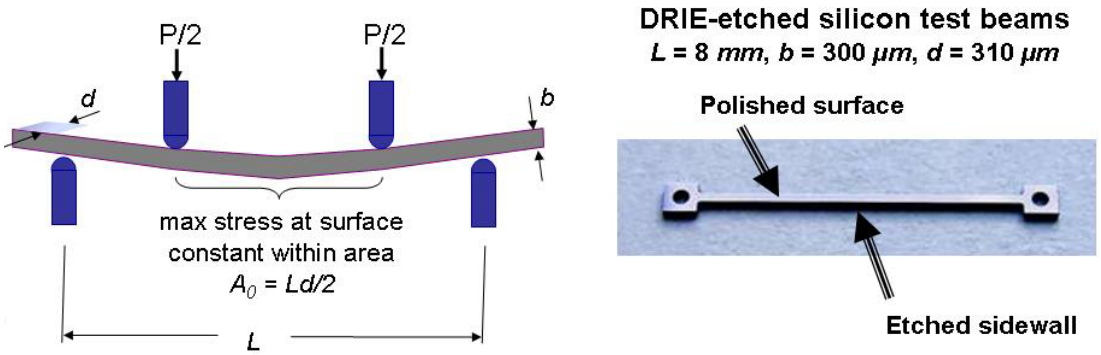


(b)

Fig. 6: SEM images of three different DRIE recipes (a) entire sidewall of specimen and (b) close-up view of the scallop

We used miniature four-point bend specimens to measure the fracture strength of the DRIE-etched silicon surfaces as well as the bare polished wafer surface perpendicular to the etched surface. Four-point bend is a standardized method to measure the strength of a surface and can be used for beams of any size (although fixturing becomes more challenging for very tiny specimens). [3] A beam under four-point load develops its maximum stress only on its outer surface, in the area between the inner load points (Figure 7) and so provides a measurement of surface strength.

The test specimens were made by etching completely through photoresist-patterned, 0.3mm thick, Prime grade double-polished silicon wafers (Figure 7). The specimens were diced out of the wafers and loaded into a custom test apparatus, which applied a compressive load to each specimen until fracture. The applied load was measured using a load cell, and converted to a fracture stress value [3]:



(a) (b)

Fig. 7: (a) Diagram of the loading and geometry of a four-point bend specimen. (b) Photograph of a silicon test beam. The beam has four surfaces, two which have been etched, and two which are a standard polished wafer surface (semiconductor Prime grade).

For each of the three DRIE recipes ("150nm," "1500nm," and "3500nm"), over 50 individual beams were fabricated, then fractured. We also fractured a group of beams on their polished surface ("Polish") to compare the strength of a standard polished wafer

surface against the etched surfaces. Finally, we had a fifth group of beams that had accidently received poor resist preparation prior to undergoing DRIE etch with the 150nm scallop etch recipe (dubbed, "Corner erosion"). During the etch, the resist mask on these samples began to prematurely erode away, which resulted in severe etch damage to the corners of the beam (i.e. the apex where the etched sidewall and top polished surface meet).

Figure 8 shows the measured fracture strength data for all test specimens, which span a very wide range, from 200MPa to 2GPa. A quick glance at these data reinforces the challenge of structural design with brittle materials; in a group of identically-manufactured specimens, some will always be quite weak and others quite strong.

A probability distribution function is helpful for describing the strength of brittle materials from a given population, and the Weibull function is widely employed for this purpose. The Weibull function can describe a population which has finite lifetime or strength; for example, at some time or load, the probability that the entire population will fail is 100%. (For more background on the Weibull function and its application to reliability testing, see references [4] and [5].)

The analysis of these data followed ASTM Standard C1239-07.[5] Fracture strength data from each of the five groups are presented as a probability plot in Figure 8. Each group was fit with the Weibull probability distribution and the resulting Weibull modulus, m, the characteristic strength, σ, and the number of specimens, N, are shown in the table to the lower right. The modulus indicates the degree of scatter in the population, where higher m would indicate more ordered, uniform material properties, and lower m indicates more randomness. The characteristic strength is defined as the stress at which 63.2% of the population would fail. The 95% confidence interval boundaries for each group are indicated by dashed lines.

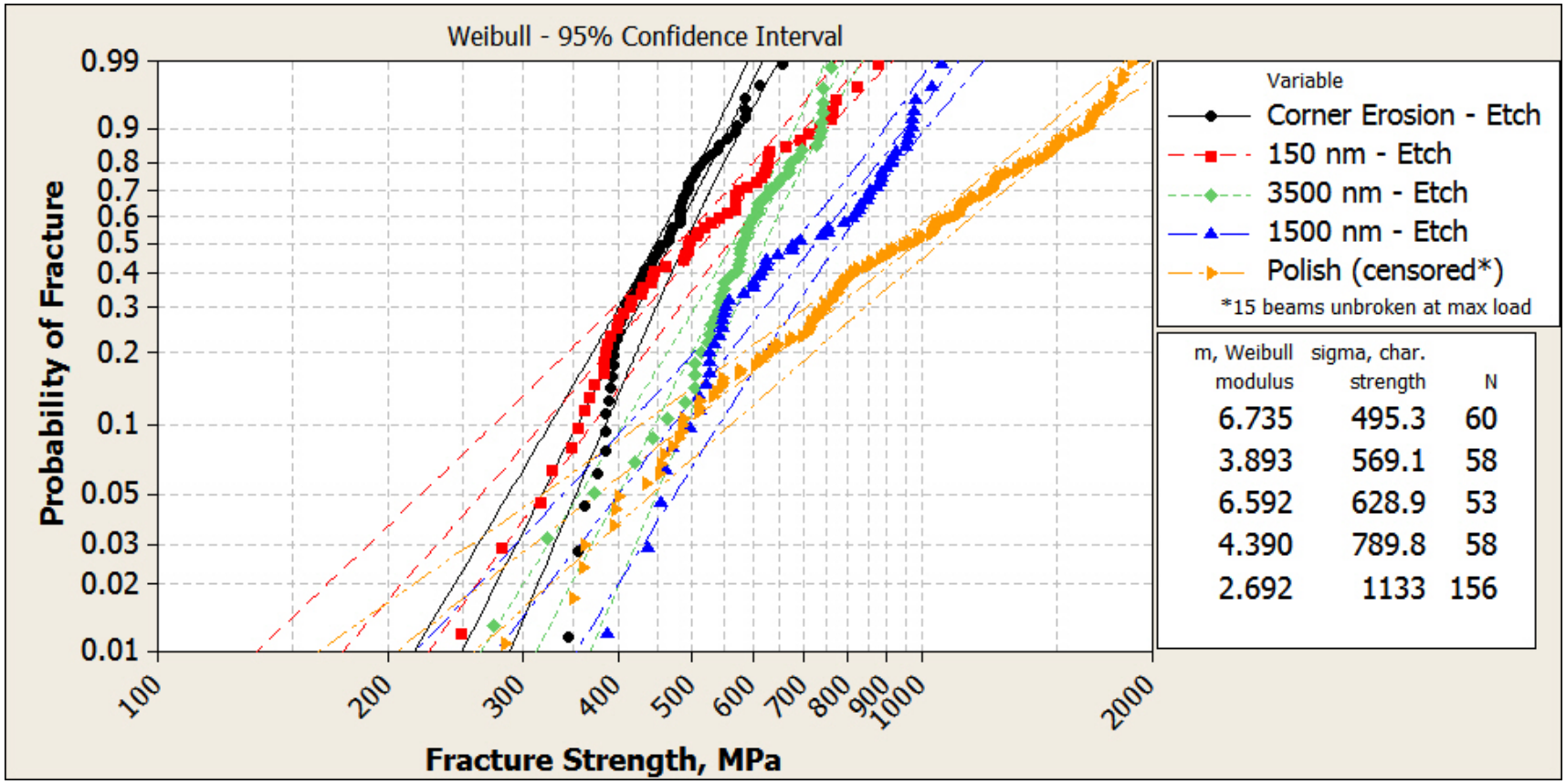


Fig. 8: Probability plot of the fracture test data from five different groups of specimens.

Several interesting results are apparent in the data. Each of the five groups are statistically distinct; their confidence intervals do not overlap. The Weibull parameters provide a quantitative description of the surface properties for each recipe. A quantitative measure provides a means for process monitoring; for example, the stability of a certain etch recipe can be evaluated by comparing the Weibull parameters from a given sample against the recipe's baseline parameters.

The characteristic strengths of the different DRIE recipes varied by 40% from the weakest to the strongest, and the "1500nm" recipe exhibited the highest value. One implication of these data is that etch recipe development, together with fracture testing, can be an effective means to improve MEMS device strength and reliability.

The polished surface had significantly higher strength, double that of the weaker etch recipes, but the lowest modulus. The etched surfaces have a higher Weibull modulus, because the induced flaws from the DRIE scallop pattern weakens the surface in a regular way, leading to more consistent fracture behavior. Polished surfaces, despite their much smaller flaws, have a more random flaw distribution, resulting in a low Weibull modulus, even though the characteristic strength is much higher.

Also of note is that the "Corner erosion" specimens that had received poor resist preparation and were etched using the 150nm recipe exhibited lower strength than the "150 nm" specimens. Micro-masking, resulting from the poor resist, significantly affected surface strength. These data indicate that masking is as significant a contributor to overall strength as etch recipe, and that process engineers must consider the effects of both in concert.

Finally, it is clear from the data that smaller scallops are not automatically better than larger scallops in terms of surface strength, as one might have hypothesized. While smaller scallops have shallower bites into the sidewall, they also result in more apexes per sidewall as compared to a large scallop recipe (see Figure 6). We were unable to

determine the fracture initiation point for these specimens, because the specimens fractured into multiple pieces as a result of four-point bend. So we can not comment on which exact feature (scallop, apex, etc.) may weaken the surface. Furthermore, the "Corner Erosion" data indicates that lithography-induced flaws, such as from micro-masking, significantly affect surface strength. We therefore recommend, from a practical standpoint, that the fracture strength data and Weibull parameters be used as the definitive metric for determining when an etch recipe is "smooth enough" – meaning "strong enough" - and process engineers should not fixate too much on sidewall appearances.

Practical Application of Strength Data

Conventional finite element (FE) simulation tools can accurately calculate stress in brittle structures, but not reliability, because the models can not include information on flaw populations (recall that brittle materials fail from the combined effect of stress and flaws). Many MEMS engineers, for lack of a better option, resort to guessing at a single failure stress value for silicon, and then compare calculated FE stress values to determine a safety factor for their designs. This is a technically unsound and dangerous approach, as evidenced by the data in Figure 8. AMFitzgerald is developing new fracture prediction software to fulfill industry need for more accurate reliability simulation tools. Our methodology is based on the combination of process-specific fracture data with traditional FE methods, and employs the test and analysis methods described above. [6]

Strength data have many uses beyond just improving device reliability, which are outlined in Table 2 below. Most significantly, this test method and strength data (i.e. Weibull parameters associated with a specific recipe) can be used to objectively compare etch performance between recipes, tools and even across foundries. Fracture strength tests could become an important part of foundry evaluation, tool purchase decisions, and process control and stability monitoring. Given the general tradeoff between etch time and sidewall smoothness, MEMS designers can use these methods to test etch recipe performance and optimize wafer throughput. Most MEMS devices fabricated today will be sold to consumer electronics OEMs, where low unit cost is paramount. DRIE etch is

one of the most expensive and slowest process steps, so optimizing recipe performance can have a significant effect on unit cost.

Table 2: Practical uses of fracture strength data

Foundry/Etch Tool Selection	• Compare fracture strengths across recipes, etch tools, foundries • Make informed purchase decisions
Cost Savings	• Informed etch recipe selection to optimize wafer throughput without sacrificing reliability • Reduce development time • Improve yield
Quality Control	• Monitor etch process stability • Across-wafer uniformity • Diagnose in-process fracture failures • Improve mechanical reliability
Design	• Reliability simulation, fracture prediction • Performance improvements • Size reduction

Summary

In this paper, we have presented the theory and methodology for objectively assessing the performance of DRIE etch recipes by measuring fracture strength of etched specimens. The methods presented here are traceable to existing ASTM standards and are simple and cost-effective to perform with a basic set of testing equipment. In this short study, we tested and measured the fracture strength of three different DRIE etch recipes and observed a difference in Weibull characteristic strength of 40% across the recipes. We also observed that lithography and masking quality contributes significantly to surface strength and should not be overlooked during process development. The data and methods presented here are also useful beyond just MEMS device reliability and can provide important objective information on tool purchases, foundry evaluation and manufacturing cost reduction.

Acknowledgements

Brent Huigens, Dawn Hilken, Carolyn White (AMFitzgerald & Associates), Geneviève Bëïque, Florent Modica (Tegal Corporation), Karl Malchar (Instron Corporation).

References

[1] Laermer, F. and Schilp, "A method of anisotropically etching silicon," US Patent 5,501,893, 26 March 1996.

[2] Blauw, M., Zijlstra, T., van der Drift, E. "Balancing the etching and passivation in time-multiplexed deep dry etching of silicon," *J. Vac. Sci. Technol. B*, Vol. 19 No. 6 Nov/Dec 2001, p. 1.

[3] ASTM Standard D 6272-02, "Standard Test Method for Flexural Properties of Unreinforced and Reinforced Plastics and Electrical Insulating Materials by Four-Point Bending," ASTM Int., West Conshohocken, PA, 2002.

[4] W. Weibull, "A statistical distribution function of wide applicability," Trans. ASME, J. Appl. Mech., vol. 18, no. 3, pp. 293–297, 1951.

[5] ASTM Standard C 1239-07, "Standard Practice for Reporting Uniaxial Strength Data and Estimating Weibull Distribution Parameters for Advanced Ceramics," ASTM Int., West Conshohocken, PA, 2007.

[6] A. M. Fitzgerald, D. M. Pierce, B. M. Huigens, and C. D. White, "A general methodology to predict the reliability of single crystal silicon MEMS devices," Journal of Microelectromechanical Systems, vol. 18, pp. 962–970, 2009.

AMFitzgerald & Associates Contact
Dr. Alissa Fitzgerald
Founder and Managing Member
+1 650-347-6367 x101
amf@amfitzgerald.com

AMFitzgerald & Associates, LLC
700 Airport Blvd. Suite 210
Burlingame, CA 94010 USA

Tegal Contact
Paul Werbaneth
VP – Marketing and Applications
+1 707-765-5608
pwerbane@tegal.com

Tegal Corporation
2201 S. McDowell Blvd.
Petaluma, CA 94954 USA
+1 707-763-5600